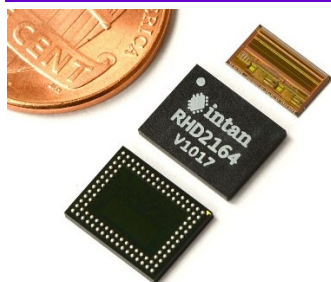# RHD2164

Digital Electrophysiology Interface Chip

5 September 2013; updated 1 December 2017

Features

♦ Fully integrated electrophysiology amplifier array with on-chip 16-bit analog-to-digital converter (ADC) and double-data-rate (DDR) serial peripheral interface (SPI)

♦ Dual on-chip ADC operation to 2.10 MSamples per second; supports sampling 64 amplifier channels at 30 kSamples/s each

♦ Low input-referred noise: 2.4 µV$_{rms}$ typical

♦ Double-data-rate (DDR) four-wire 16-bit SPI interface with CMOS or low-voltage differential signaling (LVDS) I/O pins

♦ Upper cutoff frequency of all amplifiers set by on-chip registers; adjustable from 100 Hz to 20 kHz

♦ Lower cutoff frequency of all amplifiers set by on-chip registers; adjustable from 0.1 Hz to 500 Hz

♦ Integrated multi-frequency *in situ* electrode impedance measurement capability

♦ Optional on-chip DSP high-pass filters for amplifier offset removal

♦ Auxiliary ADC inputs for interfacing additional sensors.

♦ Individual amplifier power up/down for power minimization

Applications

♦ Miniaturized multi-channel headstages for neural or ECoG recording

♦ Low-power wireless headstages or backpacks for electrophysiology experiments

♦ Recording spikes and/or local field potentials (LFPs) from microelectrodes

♦ "Smart Petri dish" *in vitro* recording systems

♦ High density neural recording systems.

Description

The Intan Technologies RHD2000-series microchips are complete low-power electrophysiology signal acquisition systems. These patent-pending devices contain arrays of low-noise amplifiers with programmable bandwidths and are suitable for a wide variety of biopotential monitoring applications. Innovative circuit architecture combines amplifiers, analog and digital filters, a multiplexed 16-bit analog-to-digital converter (ADC), and a flexible electrode impedance measurement module onto a single silicon chip. **In practice, many recording electrodes are connected directly to one side of the chip, and serial digital data exits the other side on a serial peripheral interface bus.**

The detailed operation of RHD2000-series microchips are described in the **RHD2000 series datasheet**, available on the Intan Technologies website. It is recommended that new users consult this more general datasheet along with this document, which only describes variations from the general design that are relevant for the **RHD2164**, the 64-channel version of these chips.

A low-distortion, high-speed analog multiplexer (MUX) allows a total of 64 amplifiers to share two on-chip ADCs. The ADCs can sample each channel up to 30 kSamples/s. Each chip includes three auxiliary input pins for connecting external sensors or other analog voltages which may be sampled using the ADC. Additional on-chip circuitry enables *in situ* electrode impedance measurements at user-programmable frequencies. By transforming weak electrode signals directly into a digital data stream, **the RHD2164 replaces all analog instrumentation circuitry** in electrophysiology monitoring and acquisition systems.

RHD2164 chips are packaged in 9.0 mm × 7.0 mm BGA surface-mount packages weighing 0.15 grams, or available in 7.3 mm × 4.2 mm bare die for chip-on-board assembly. The small footprint of this chip enables the miniaturization of front end electronics for miniature headstages and other wearable or portable biopotential recording systems.

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RHD2000 Series Family

There are three devices in the RHD2000-series electrophysiology interface family: the RHD2216, RHD2132, and RHD2164. The following table lists the features of these chips:

| DEVICE	AMPLIFIERS PER CHIP	AMPLIFIER INPUT PINS	SMD PACKAGE SIZE	BARE DIE SIZE
RHD2216	16	16 × 2 differential amplifier inputs	8 mm × 8 mm 56-pin QFN	4.8 mm × 4.1 mm
RHD2132	32	32 unipolar amplifier inputs; 1 common reference input	8 mm × 8 mm 56-pin QFN	4.8 mm × 4.1 mm
RHD2164	64	64 unipolar amplifier inputs; 1 common reference input	9 mm × 7 mm 104-pin BGA	7.3 mm × 4.2 mm

The positive and negative amplifier inputs on the RHD2216 have balanced input impedances; this will provide the best rejection of common-mode noise (most commonly, 50/60 Hz interference) if all electrodes, including reference electrodes, are roughly the same impedance. This is usually the case for surface EMG, EKG, and EEG recording.

The RHD2132 or RHD2164 can be used in applications where the reference electrode has a much different impedance than the recording electrodes (e.g., microelectrodes for neural recording with a platinum of Ag/AgCl reference wire) or in cases where common-mode noise will not be severe (e.g., implanted devices). The common reference input (**ref_elec**) is connected to the negative input of all amplifiers, and therefore has an input impedance many times lower than the individual amplifier inputs.

Package Dimensions

9 mm × 7 mm 104-Pin BGA package (0.5-mm pitch) – all dimensions in millimeters

BOTTOM VIEW

SIDE VIEW

seating plane

TOP VIEW
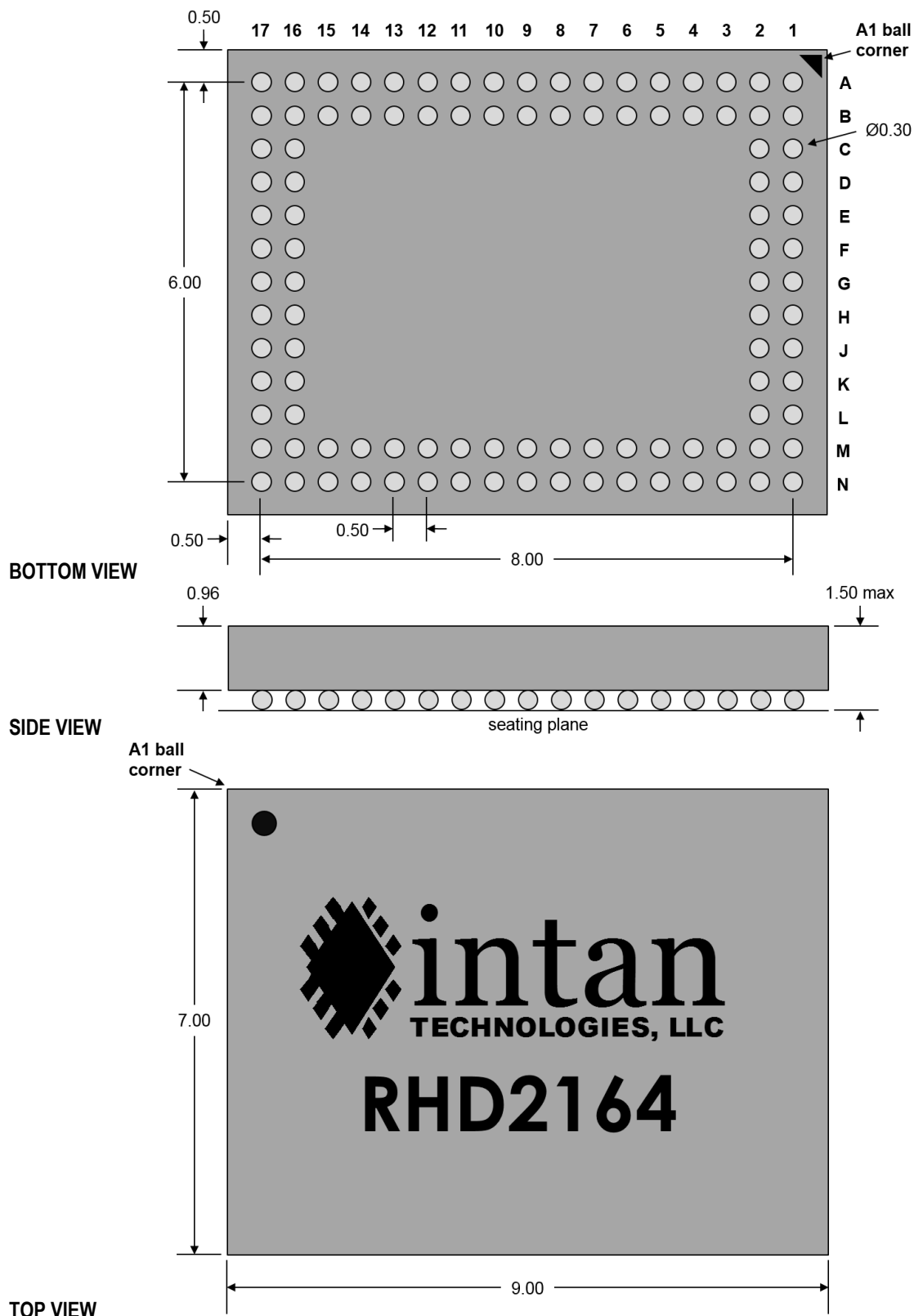
Pin Locations

PIN	NAME	TYPE	PIN	NAME	TYPE
A1	in16	analog input	E1	in9	analog input
A2	in18	analog input	E2	in10	analog input
A3	in20	analog input	E16	in53	analog input
A4	in22	analog input	E17	in54	analog input
A5	in24	analog input	F1	in7	analog input
A6	in26	analog input	F2	in8	analog input
A7	in28	analog input	F16	in55	analog input
A8	in30	analog input	F17	in56	analog input
A9	in32	analog input	G1	in5	analog input
A10	in33	analog input	G2	in6	analog input
A11	in35	analog input	G16	in57	analog input
A12	in37	analog input	G17	in58	analog input
A13	in39	analog input	H1	in3	analog input
A14	in41	analog input	H2	in4	analog input
A15	in43	analog input	H16	in59	analog input
A16	in45	analog input	H17	in60	analog input
A17	in47	analog input	J1	in1	analog input
B1	in15	analog input	J2	in2	analog input
B2	in17	analog input	J16	in61	analog input
B3	in19	analog input	J17	in62	analog input
B4	in21	analog input	K1	nc	not connected
B5	in23	analog input	K2	in0	analog input
B6	in25	analog input	K16	in63	analog input
B7	in27	analog input	K17	nc	not connected
B8	in29	analog input	L1	nc	not connected
B9	in31	analog input	L2	nc	not connected
B10	in34	analog input	L16	nc	not connected
B11	in36	analog input	L17	elec_test	analog input
B12	in38	analog input	M1	ref_elec	analog input
B13	in40	analog input	M2	VESD	power
B14	in42	analog input	M3	nc	not connected
B15	in44	analog input	M4	nc	not connected
B16	in46	analog input	M5	nc	not connected
B17	in48	analog input	M6	nc	not connected
C1	in13	analog input	M7	nc	not connected
C2	in14	analog input	M8	nc	not connected
C16	in49	analog input	M9	nc	not connected
C17	in50	analog input	M10	nc	not connected
D1	in11	analog input	M11	nc	not connected
D2	in12	analog input	M12	nc	not connected
D16	in51	analog input	M13	nc	not connected
D17	in52	analog input	M14	nc	not connected

Pin Locations

PIN	NAME	TYPE
M15	VDD	power
M16	LVDS_en	digital input
M17	GND	power
N1	GND	power
N2	VDD	power
N3	auxin1	analog input
N4	auxin2	analog input
N5	auxin3	analog input
N6	GND	power
N7	$\overline{CS}$–	digital input
N8	$\overline{CS}$+	digital input
N9	SCLK–	digital input
N10	SCLK+	digital input
N11	MOSI–	digital input
N12	MOSI+	digital input
N13	MISO–	digital output
N14	MISO+	digital output
N15	VDD	power
N16	auxout	digital output
N17	ADC_ref	analog output

Printed Circuit Board Layout

The PCB footprint for the BGA package should use round pads with a diameter of 250 µm (10 mils). There should be a circular solder mask opening with 50 µm (2 mil) clearance around each pad.

The PCB will need to use a maximum trace width of approximately 75 µm (3 mils) in order to route signals between adjacent BGA pins.

There are three ground pads and three power pads (labeled **GND** and **VDD**). **All six** of these pads **must** be connected to the appropriate supply voltages for proper operation. An off-chip 100 nF capacitor between ground and VDD should be placed less than 1 cm from the lower edge of the chip. For best operation, this capacitor should have an X5R or X7R dielectric and should be rated for at least 16V. If non-LVDS (standard CMOS) signaling is used, it is recommended that two 100 nF capacitors be used: one near the lower left corner of the chip and one near the lower right corner of the chip.

Intan suggests that all 'nc' pins (with no internal connection to the chip) be tied to ground (GND) to provide lateral shielding between sensitive analog input pins and noisy digital I/O pins on the circuit board.

The **ADC_ref** pin must be connected to an off-chip 10 nF capacitor to ground, which should be placed within 1 cm of the lower edge the chip. This capacitor should have an X5R, X7R, C0G, or NP0 dielectric and should be rated for at least 16V. If multiple RHD2164 chips are used, each chip must have its own 10 nF capacitor. The **ADC_ref** pins of different chips should not be connected.

The **VESD** pad must be connected either to ground (recommended) or to VDD. See the "Amplifier Input Protection" section of the RHD2000 series datasheet for more information on this pin.

It is not necessary to connect the **auxin1**, **auxin2**, or **auxin3** pins if auxiliary analog signals will not be connected to the chip. It is not necessary to connect the **auxout** pin of the auxiliary digital output will not be used.

In most applications, the **elec_test** pad should remain unconnected. This pad is typically used only to provide DC voltages for the purposes of electrode activation or electroplating. See the "Electrode Activation" section of the RHD2000 series datasheet for more details.

The **LVDS_en** pad of the RHD2164 chip has an internal pull-up resistor that enables LVDS signaling on the SPI bus if this pad is left unconnected. If non-LVDS (standard CMOS) SPI signaling is desired then this pad must be connected to ground.

If LVDS SPI signaling will be used, than all eight SPI pads ($\overline{CS}$–, $\overline{CS}$+, **SCLK–**, **SCLK+**, **MOSI–**, **MOSI+**, **MISO–**, **MISO+**) must be connected. If non-LVDS (standard CMOS) SPI signaling will be used, the negative SPI pins ($\overline{CS}$–, **SCLK–**, **MOSI–**, **MISO–**) can remain unconnected.

If LVDS signaling is used, 100 Ω termination resistors for $\overline{CS}$, SCLK, and MOSI should be placed within 20 cm of the chip. The 100 Ω termination resistor for MISO should be placed near the controller and will likely not reside on the same board as the RHD2000. (Many LVDS receivers and FPGAs have built-in termination resistors, so this device may not be necessary.)

BGA Package Materials

The material composition of the solder balls on the bottom of the BGA package is SAC305, a lead-free alloy composed of 96.5% tin, 3% silver, and 0.5% copper. It has a low melting point of 217° - 218°C (423° - 424°F).

A rerouting circuit board inside the BGA contains small amounts of nickel, a ferromagnetic metal.

Die Diagram

Each RHD2164 bare die is approximately 7.3 mm × 4.2 mm in size, though the size may vary slightly from die to die due to variations in sawing. Each chip is approximately 0.20 mm thick.

The following diagram shows the location of bond pads on the RHD2164 die, relative to the center of the die. Dimensions are in microns. The gray rectangle marks the approximate outline of the die. The highly visible top layers of metal are shown in green and blue. The bond pads are shown in red.
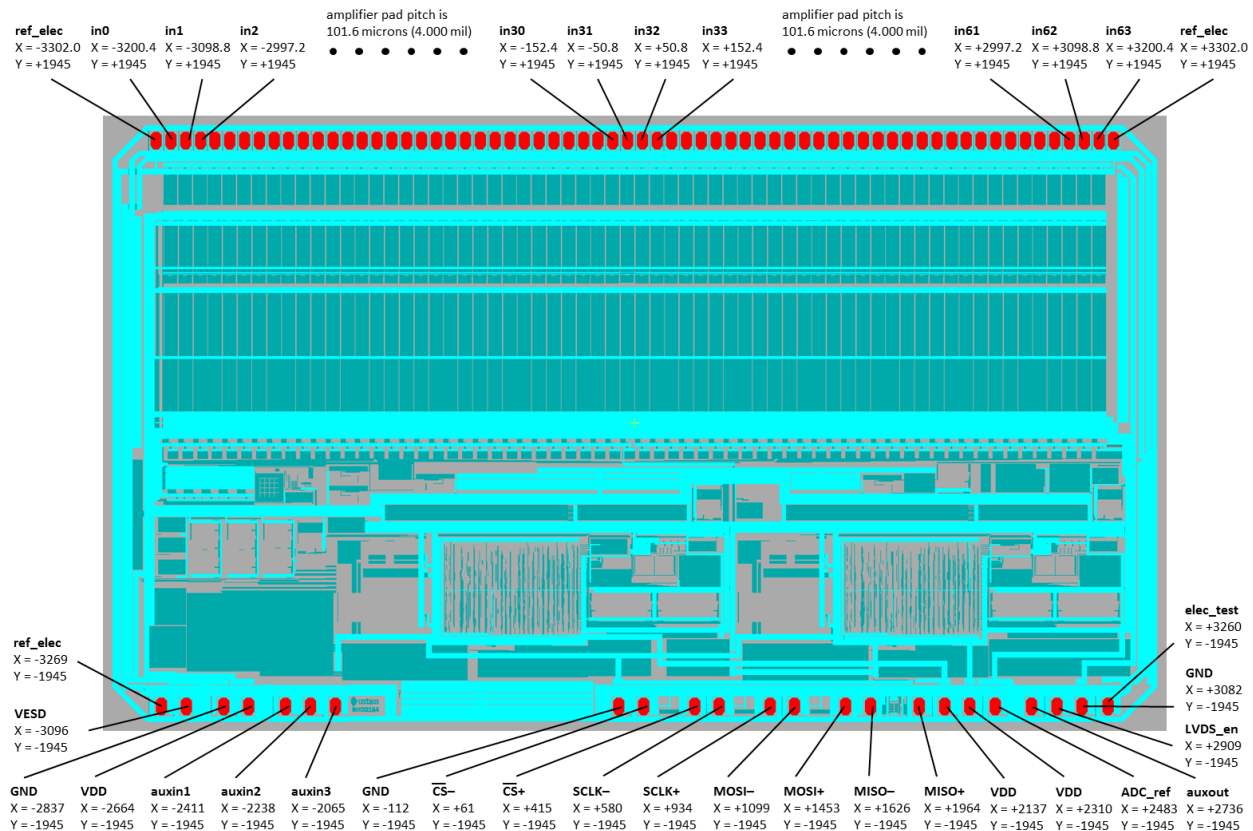
The dimensions of each bond pad are shown at the right (in microns). The bond pad metal is AlCu: 99.5% aluminum, 0.5% copper.

The bond pads along the top edge of the chip are spaced 101.6 µm apart, or 4.000 mil (1 mil = 0.001 inch). This pitch was chosen to be compatible with advanced printed circuit board (PCB) technology that allows for conductive traces with a width of 2 mil and a trace-to-trace spacing of 2 mil.
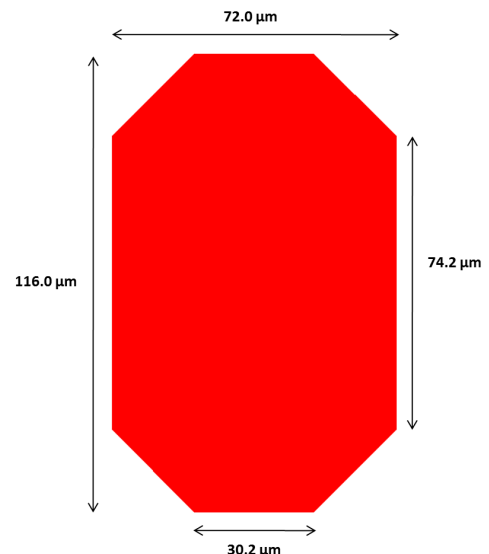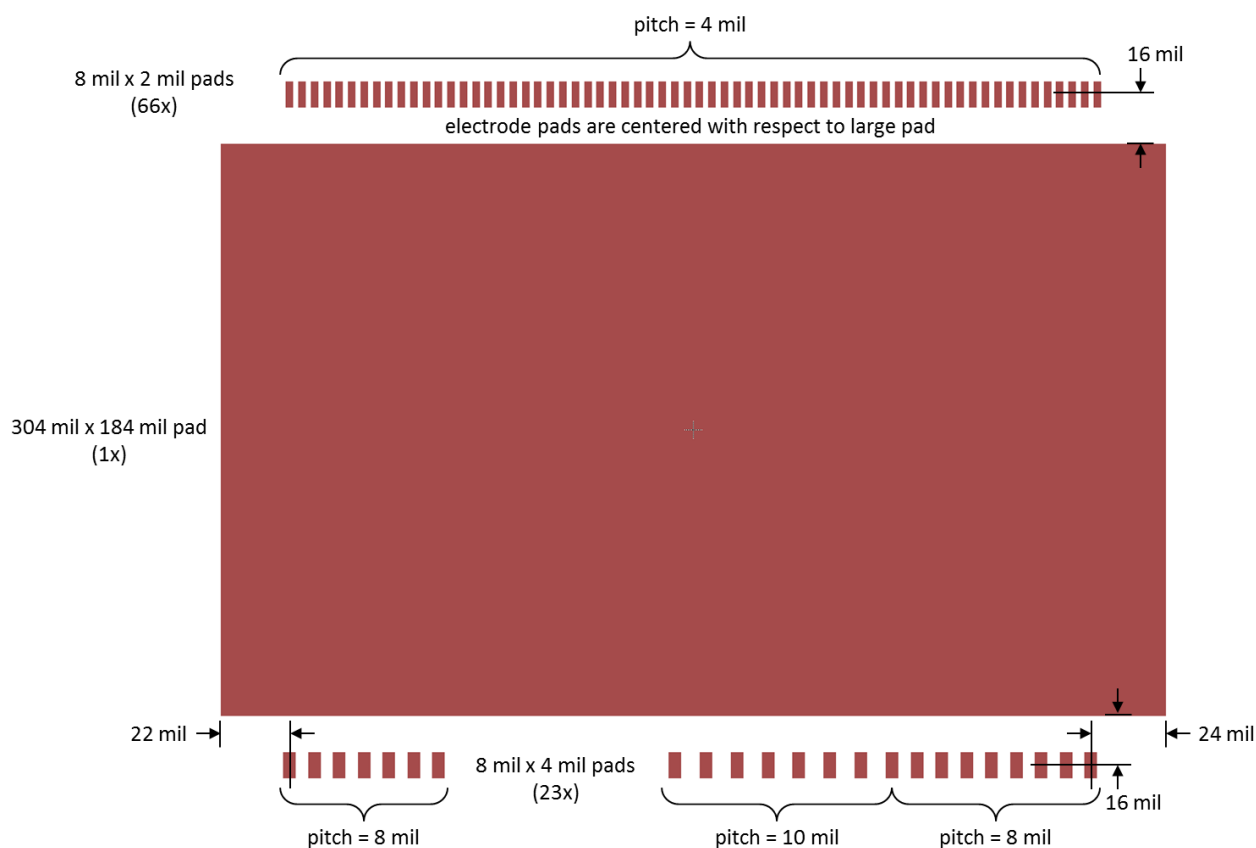
Suggested PCB Footprint for Chip-on-Board Assembly

A sample PCB footprint for chip-on-board assembly of the RHD2164 is shown in the following diagram, and is available from Intan Technologies in Eagle PCB library format. However, it is recommended that users review their bonding capabilities to ensure that bond wire lengths and other assembly factors are compatible with the layout provided. Generally, it is recommended to draw a large metal pad for the chip that is slightly larger than the die, and to tie this to ground. The PCB pads for connecting the bond wires from the chip are typically centered approximately 0.65 mm (25 mil) from the top or bottom edge of the chip.

Dimensions are given in mils, where 1 mil = 0.001 inch = 25.4 microns. To facilitate chip-on-board assembly, PCBs should have a planar surface finish of soft bondable gold or ENIG immersion gold.

The large pad underneath the chip serves two purposes: By connecting this to ground, it shields the chip electrically from underneath, and it also shields the bottom of the chip from light. All silicon chips are light-sensitive, and most PCBs are translucent, so a solid piece of metal is needed to prevent 100/120 Hz noise pick-up from 50/60 Hz AC lighting. After bonding, the chip and bond wires should be covered with opaque epoxy for protection from mechanical impact and from light.

pitch = 4 mil

16 mil

8 mil x 2 mil pads
(66x)

electrode pads are centered with respect to large pad

304 mil x 184 mil pad
(1x)

22 mil

8 mil x 4 mil pads
(23x)

24 mil

16 mil

pitch = 8 mil

pitch = 10 mil

pitch = 8 mil

Notes on Optional Bond Wires and Chip-on-Board Design

Each RHD2164 die has three bondpads for the reference electrode connection (labeled **ref_elec**). These are located in the upper left, upper right, and lower left corners of the chip. These pads are connected internally on the chip, so only **one** of these pads needs to be bonded. There is no advantage to bonding more than one of these pads. Multiple bond pads are provided only for circuit board layout convenience.

There are three ground pads and three power pads (labeled **GND** and **VDD**). **All six** of these pads **must** be bonded and connected to the appropriate supply voltages for proper operation. An off-chip 100 nF capacitor between ground and VDD should be placed less than 1 cm from the lower edge of the chip. For best operation, this capacitor should have an X5R or X7R dielectric and should be rated for at least 16V. If non-LVDS (standard CMOS) signaling is used, it is recommended that two 100 nF capacitors be used: one near the lower left corner of the chip and one near the lower right corner of the chip.

The **ADC_ref** pin must be bonded and connected to an off-chip 10 nF capacitor to ground, which should be placed within 1 cm of the lower edge the chip. This capacitor should have an X5R, X7R, C0G, or NP0 dielectric and should be rated for at least 16V. If multiple RHD2164 chips are used, each chip must have its own 10 nF capacitor. The **ADC_ref** pins of different chips should not be connected.

The **VESD** pad must be bonded and connected either to ground (recommended) or to VDD. See the "Amplifier Input Protection" section of the RHD2000 series datasheet for more information on this pin.

It is not necessary to bond the **auxin1**, **auxin2**, or **auxin3** pins if auxiliary analog signals will not be connected to the chip.

It is not necessary to bond the **auxout** pin of the auxiliary digital output will not be used.

In most applications, the **elec_test** pad should remain unbonded. This pad is typically used only to provide DC voltages for the purposes of electrode activation or electroplating. See the "Electrode Activation" section of the RHD2000 series datasheet for more details.

The **LVDS_en** pad of the RHD2164 chip has an internal pull-up resistor that enables LVDS signaling on the SPI bus if this pad is left unbonded. If non-LVDS (standard CMOS) SPI signaling is desired then this pad must be bonded and connected to ground.

If LVDS SPI signaling will be used, than all eight SPI pads ($\overline{\text{CS}}$**–**, $\overline{\text{CS}}$**+**, **SCLK–**, **SCLK+**, **MOSI–**, **MOSI+**, **MISO–**, **MISO+**) must be bonded. If non-LVDS (standard CMOS) SPI signaling will be used, the negative SPI pins ($\overline{\text{CS}}$**–**, **SCLK–**, **MOSI–**, **MISO–**) can remain unbonded.

If LVDS signaling is used, 100 Ω termination resistors for $\overline{\text{CS}}$, SCLK, and MOSI should be placed within 20 cm of the chip. The 100 Ω termination resistor for MISO should be placed near the controller and will likely not reside on the same board as the RHD2000. (Many LVDS receivers and FPGAs have built-in termination resistors, so this device may not be necessary.)

RHD2164 Simplified Diagram

The RHD2164 contains an array of 64 amplifiers having unipolar inputs (**in0**, **in1**,...) and a common, shared reference line (**ref_elec**).

Each RHD2164 contains two 32-channel modules (essentially two RHD2132 cores) working in parallel, each with its own analog multiplexer and ADC. The A module consists of amplifier channels 0-31, and the B module consists of amplifier channels 32-63. The A and B modules receive the same commands from the MOSI line. If a command is sent to convert amplifier channel X, then the A module converts amplifier channel X and the B module simultaneously converts amplifier channel X+32.

The 16-bit results from the two ADCs (conveyed serially on the MISO A and MISO B lines) are combined into a single MISO signal by a double data rate (DDR) multiplexer. The operation of this module is described on the following page.

A shown below the auxiliary analog inputs, on-chip temperature sensor, and supply voltage sensor are connected only to the A module. When an ADC conversion is performed on one of these non-amplifier channels, the result from the B module is meaningless and should be ignored.
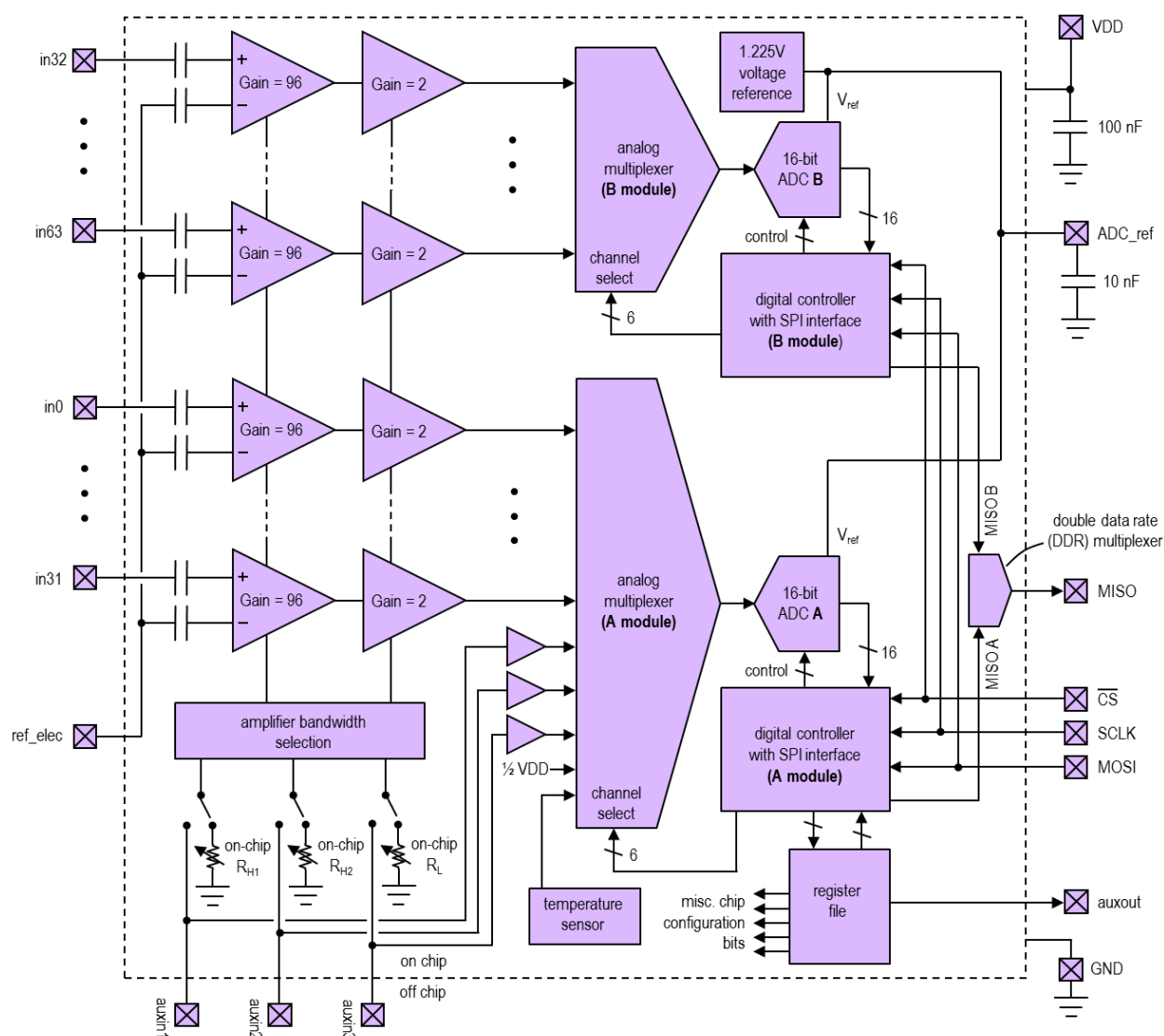
Double Data Rate (DDR) Multiplexer

The block diagram below shows the circuit used in the RHD2164 to merge two serial data signals (MISO A and MISO B) into one double-data-rate (DDR) MISO signal. Two D flip-flops are clocked with complementary signals to synchronize the data with rising or falling SCLK edges. A digital multiplexer alternately selects data from MISO A and MISO B to merge the two serial data streams.
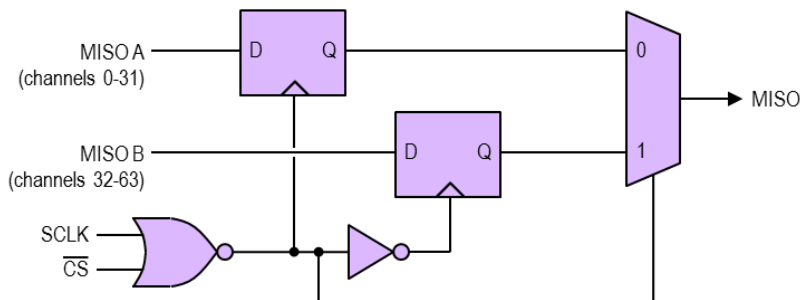

Double Data Rate (DDR) SPI Bus Signals

Like the 16-channel RHD2216 and 32-channel RHD2132, the 64-channel RHD2164 chip communicates using an SPI interface consisting of four signals: an active-low chip select ($\overline{CS}$); a serial data clock (SCLK) with a base value of zero; a "Master Out, Slave In" data line (MOSI) to receive commands from the master device; and a "Master In, Slave Out" data line (MISO) to send pipelined results from prior commands to the master device. The RHD2164 chip always functions as the SPI slave device.

During each chip select cycle, a 16-bit command word is transferred to the chip, MSB first. As shown on the following page, the RHD2164 samples MOSI on the rising edge of SCLK. A double data rate (DDR) technique is used to transfer 32 bits of data back during the same chip select cycle. The master should sample MISO on the rising **and** falling edges of SCLK, and on the rising edge of $\overline{CS}$ (see timing diagram on following page). The data present on MISO during the falling edges of SCLK convey the 16-bit data from the MISO A signal (i.e., amplifier channels 0-31). The data present on MISO during the first rising edge of SCLK should be ignored. The data on successive SCLK rising edges convey the first 15 bits of data from the MISO B module (i.e., amplifier channels 32-63). The 16th bit (LSB) of data from the B module is conveyed on the rising edge of $\overline{CS}$.

Note that this DDR technique is a non-standard mode of SPI communication and will likely require an FPGA to implement. The open-source Rhythm interface available from Intan Technologies includes Verilog code to capture DDR SPI signals and add variable delays to account for cable propagation delays. See the **RHD2000 USB/FPGA interface datasheet** on the Intan Technologies website for more details.

The RHD2164 ADC samples the selected analog signal on the falling edge of $\overline{CS}$. The $\overline{CS}$ line must be pulsed high between every 16-bit data transfer, even when the command word does not request an analog-to-digital conversion.

DDR Timing Diagram
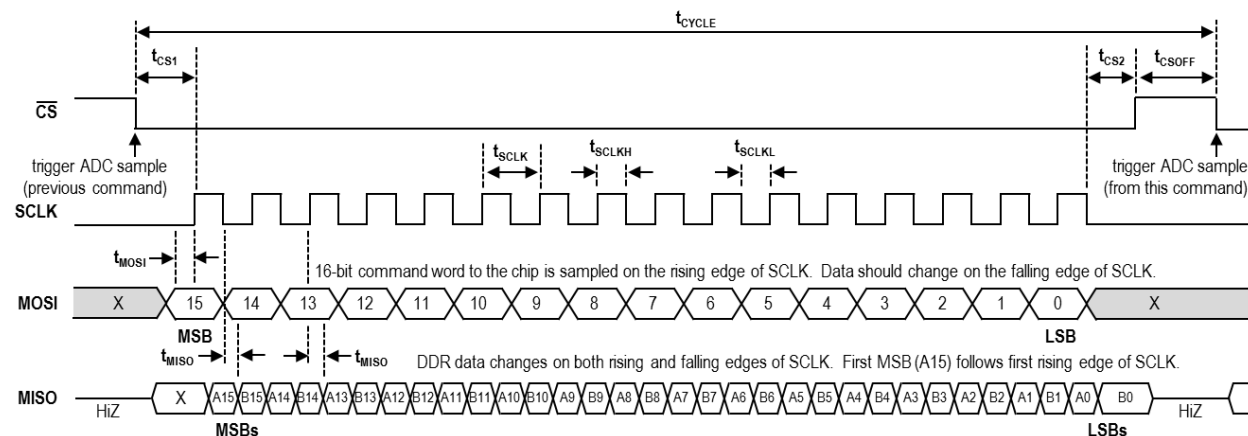
SPI BUS TIMING SPECIFICATIONS

T_A = 25ºC, V_{DD} = 3.3V unless otherwise noted.

SYMBOL	PARAMETER	MIN	MAX	UNIT	COMMENTS
t_{SCLK}	SCLK Period	41.6		ns	Maximum SCLK frequency is 24 MHz
t_{SCLKH}	SCLK Pulse Width High	20.8		ns	
t_{SCLKL}	SCLK Pulse Width Low	20.8		ns	
t_{CS1}	$\overline{CS}$ Low to SCLK High Setup	20.8		ns	
t_{CS2}	SCLK Low to $\overline{CS}$ High Setup	20.8		ns	
t_{CSOFF}	$\overline{CS}$ High Duration	154		ns	
t_{MOSI}	MOSI Data Valid to SCLK High Setup	10.4		ns	
t_{MISO}	SCLK or $\overline{CS}$ Falling Edge to MISO Data Valid		12	ns	
t_{CYCLE}	Total Cycle Time Between ADC Samples	950		ns	Maximum sample rate is 1.05 MS/s per 32-channel module, or 30 kS/s per channel for all 64 amplifier channels plus 3 auxiliary channels.

# Typical Connection Diagram

64-CHANNEL HEADSTAGE EXAMPLE

The diagram below shows a typical circuit schematic for a single RHD2164 chip interfaced to a controller over a long SPI interface cable. In addition to the chip, only two SMD (surface mount device) capacitors and three LVDS termination resistors are required for a complete biopotential recording front end. The 0-Ω resistor shorting **ref_elec** to ground is optional.
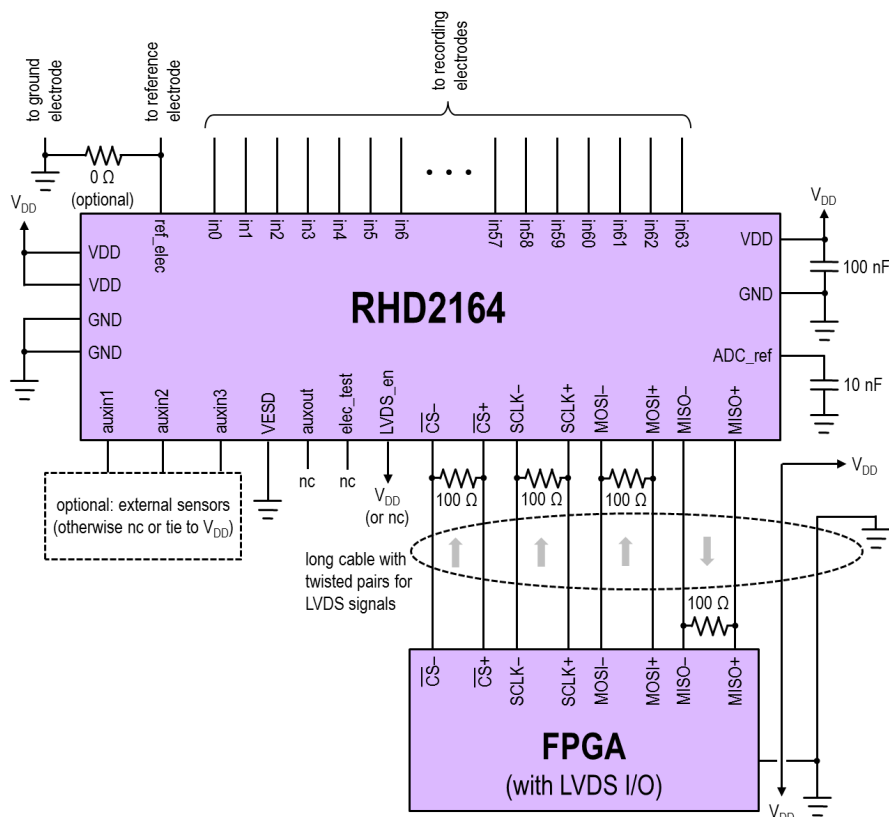
128-CHANNEL HEADSTAGE EXAMPLE

Two RHD2164 chips can share one 12-conductor SPI interface cable by receiving the same commands, as shown in the simplified diagram below. In addition to the resistors shown, each RHD2164 chip will need its own 100 nF capacitor from **VDD** to **GND** and 10 nF capacitor from **ADC_ref** to **GND**, for a total of seven SMD passive components.
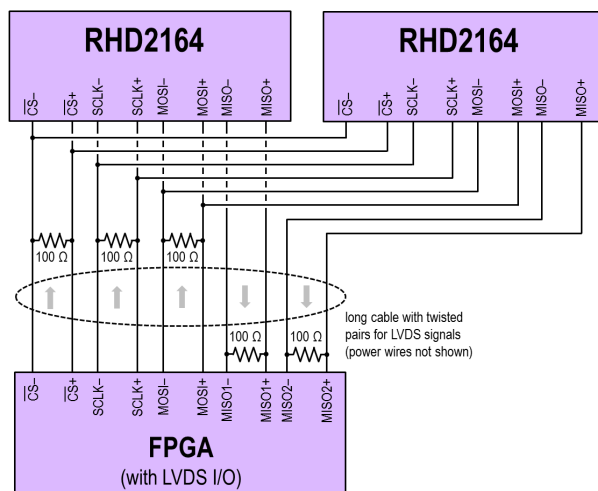
On-Chip Registers

Each RHD2164 chip is capable of addressing up to 64 eight-bit registers, in any combination of writable (RAM) registers and read-only (ROM) registers. **Upon power-up, all RAM registers contain indeterminate data and should be promptly configured by the SPI master device.** Initialization of registers should be completed at least 100 µs **before** ADC calibration as some registers set parameters that optimize ADC operation.

The RAM registers present in each RHD2164 are identical to the registers on the RHD2132 and RHD2216 chips with the few exceptions listed below. The detailed functions of the remaining registers are documented in the **RHD2000 series datasheet**, available at the Intan Technologies website.

Register 7: Impedance Check Amplifier Select

bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Register 7	X	X	Zcheck select [5:0]					

Zcheck select [5:0]: This variable selects the amplifier whose electrode will be connected to the on-chip impedance testing circuitry if **Zcheck en** is set to one. In the RHD2164, all six bits of this register are used. Although the 64 amplifiers are divided between two analog multiplexers and are sampled by the two on-chip ADCs in pairs (e.g., channel 0 and channel 32 are sampled simultaneously when a CONVERT(0) command is sent), impedance checking is performed only on one channel at a time.

Registers 14-21: Individual Amplifier Power

bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Register 14	apwr[7]	apwr[6]	apwr[5]	apwr[4]	apwr[3]	apwr[2]	apwr[1]	apwr[0]
Register 15	apwr[15]	apwr[14]	apwr[13]	apwr[12]	apwr[11]	apwr[10]	apwr[9]	apwr[8]
Register 16	apwr[23]	apwr[22]	apwr[21]	apwr[20]	apwr[19]	apwr[18]	apwr[17]	apwr[16]
Register 17	apwr[31]	apwr[30]	apwr[29]	apwr[28]	apwr[27]	apwr[26]	apwr[25]	apwr[24]
Register 18	apwr[32]	apwr[33]	apwr[34]	apwr[35]	apwr[36]	apwr[37]	apwr[38]	apwr[39]
Register 19	apwr[40]	apwr[41]	apwr[42]	apwr[43]	apwr[44]	apwr[45]	apwr[46]	apwr[47]
Register 20	apwr[48]	apwr[49]	apwr[50]	apwr[51]	apwr[52]	apwr[53]	apwr[54]	apwr[55]
Register 21	apwr[56]	apwr[57]	apwr[58]	apwr[59]	apwr[60]	apwr[61]	apwr[62]	apwr[63]

apwr [63:0]: Setting these bits to zero powers down individual biopotential amplifiers, saving power if there are channels that don't need to be observed. Each amplifier consumes power in proportion to its upper cutoff frequency. Current consumption is approximately 7.6 µA/kHz per amplifier. Under normal operation, these bits should be set to one.

Registers 18-21 do not exist on the RHD2216 or RHD2132 chips. The contents of these RHD2164-specific registers may be set using the traditional WRITE command. However, if a READ command is sent to read back the contents of Registers 18-21, the results will only appear correctly on the MISO B data stream. The results of all other registers should be read from the MISO A data stream. In most applications it is probably not necessary to read the contents of these registers; when they are modified, copies of their most recent values may be stored on the controller.

On-Chip Read-Only Registers

Each RHD2164 chip contains the following ROM registers that provide information on the identity and capabilities of the particular chip.

Registers 40-44: Company Designation

The read-only registers 40-44 contain the characters INTAN in ASCII. The contents of these registers can be read to verify the fidelity of the SPI interface.

Register 59: MISO A/B Marker

bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Register 59				MISO A/B marker [7:0]				

MISO A/B marker [7:0]: This read-only variable returns 00110101 (decimal 53) on MISO A and 00111010 (decimal 58) on MISO B. These distinct bytes can be checked by the SPI master device to confirm signal integrity on the SPI bus (e.g., to adjust internal sampling times to compensate for cable propagation delay).

Register 60: Die Revision

bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Register 60				die revision [7:0]				

die revision [7:0]: This read-only variable encodes a die revision number which is set by Intan Technologies to encode various versions of a chip.

Register 61: Unipolar/Bipolar Amplifiers

bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Register 61				unipolar [7:0]				

unipolar [7:0]: This read-only variable is set to zero if the on-chip biopotential amplifiers have independent differential (bipolar) inputs like the RHD2216 chip. It is set to one if the amplifiers have unipolar inputs and a common reference, like the RHD2132 chip or RHD2164 chip.

Register 62: Number of Amplifiers

bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Register 62				number of amps [7:0]				

number of amps [7:0]: This read-only variable encodes the total number of biopotential amplifiers on the chip (i.e., 64).

Register 63: Intan Technologies Chip ID

bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Register 63				chip ID [7:0]				

chip ID [7:0]: This read-only variable encodes a unique Intan Technologies ID number indicating the type of chip. The chip ID for the RHD2164 is 4.

Power Dissipation

Total power dissipation of a RHD2164 chip depends on how it is configured and operated. Following is a list of guidelines for estimating total supply current under various operating conditions.

Baseline amplifier array current: The amplifier array on each RHD2164 pulls 200 μA of quiescent current to power various voltage references and bias current generators.

Amplifiers: Each amplifier consumes current in proportion to its upper cutoff frequency, approximately 7.6 μA/kHz per amplifier.

Baseline ADC current: The two ADCs on the RHD2164 chip pull a total of 840 μA of quiescent current to power various voltage references and bias current generators. (This baseline level may be reduced by 180 μA by setting **amp Vref enable** to zero, and by another 160 μA by setting **ADC comparator bias** to zero, but the ADCs will be unusable with these settings.)

ADC and MUX dynamic current: The dual ADC/MUX assembly consumes additional current in proportion to the total sampling rate (individual amplifier sample rate multiplied by number of channels sampled), approximately 2.14 μA/(kS/s).

DSP high-pass filter: The DSP offset removal filter does not consume significant power.

LVDS I/O: If **LVDS_en** is pulled high to enable on-chip LVDS driver and receivers, the chip pulls an additional 5700 μA with 3.3V VDD (4740 μA with 3.0V VDD). Current draw with standard CMOS signaling is proportional to SPI data rate and MISO wire capacitance; for low data rates and short wires, it is very small.

Impedance measurement module: With **Zcheck DAC power** set to one, the DAC used for impedance testing consumes 120 μA.

Temperature sensor: Under normal operation, the temperature sensor consumes roughly 70 μA.

Supply voltage sensor and auxiliary ADC inputs: When enabled, each of these extra inputs to the ADC consumes roughly 10 μA, though this number is somewhat proportional to ADC sampling rate.

Using these guidelines, we can now estimate whole-chip power dissipation for various electrophysiology recording applications. In the examples listed here, we assume that in addition to the 64 amplifiers, an additional 3 auxiliary sensors are sampled every sampling period.

Example: Neural recording headstage 1

RHD2164
f_H **= 10 kHz**
sample rate = 67 × 30 kS/s/channel = 2.01 MS/s

Baseline amplifier array current: 200 μA
Amplifiers: 64 × 7.6 μA/kHz × 10 kHz = 4864 μA
Baseline ADC current: 840 μA
ADC/MUX: 2.14 μA/(kS/s) × 2.01 MS/s = 4301 μA
LVDS I/O: 5700 μA
Impedance measurement: 120 μA
Temperature sensor: 70 μA
Supply voltage, auxiliary inputs: 4 × 10 μA = 40 μA

Total supply current: 16.1 mA
Total power dissipation: 16.1 mA × 3.3 V = 53.1 mW

Example: Neural recording headstage 2

RHD2164
f_H **= 7.5 kHz**
sample rate = 67 × 20 kS/s/channel = 1.34 MS/s

Baseline amplifier array current: 200 μA
Amplifiers: 64 × 7.6 μA/kHz × 7.5 kHz = 3648 μA
Baseline ADC current: 840 μA
ADC/MUX: 2.14 μA/(kS/s) × 1.34 MS/s = 2868 μA
LVDS I/O: 5700 μA
Impedance measurement: 0 (usually turned off)
Temperature sensor: 0 (turned off)
Supply voltage sensor: 10 μA

Total supply current: 13.3 mA
Total power dissipation: 13.3 mA × 3.3 V = 43.9 mW

Example: ECoG recording front-end

RHD2164
f_H **= 1 kHz**
sample rate = 67 x 2 kS/s/channel = 134 kS/s

Baseline amplifier array current: 200 μA
Amplifiers: 64 × 7.6 μA/kHz × 1 kHz = 486 μA
Baseline ADC current: 840 μA
ADC/MUX: 2.14 μA/(kS/s) × 134 kS/s = 287 μA
LVDS I/O: off (assume nearby microcontroller)
Impedance measurement: 120 μA
Temperature sensor: 70 μA
Supply voltage, auxiliary inputs: 4 × 10 μA = 40 μA

Total supply current: 2.04 mA
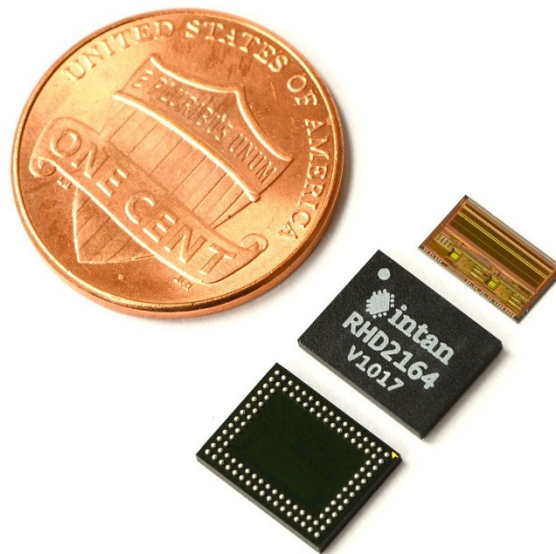**Total power dissipation: 2.04 mA × 3.3 V = 6.7 mW**

Pricing Information

See **www.intantech.com** for current pricing. All price information is subject to change without notice. Quantities may be limited. All orders are subject to current pricing at time of acceptance by Intan Technologies. Additional charges may apply for international purchases and shipping.

Contact Information

This datasheet is meant to acquaint engineers and scientists with the general characteristics of the RHD2164 digital electrophysiology interface chip developed at Intan Technologies. We value feedback from potential end users.

For more information, contact Intan Technologies at:

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Document Revision History

5 September 2013:

♦   Original document released.

2 December 2013:

♦   Added suggested PCB footprint for chip-on-board assembly.

1 December 2017:

♦   Added BGA package information.