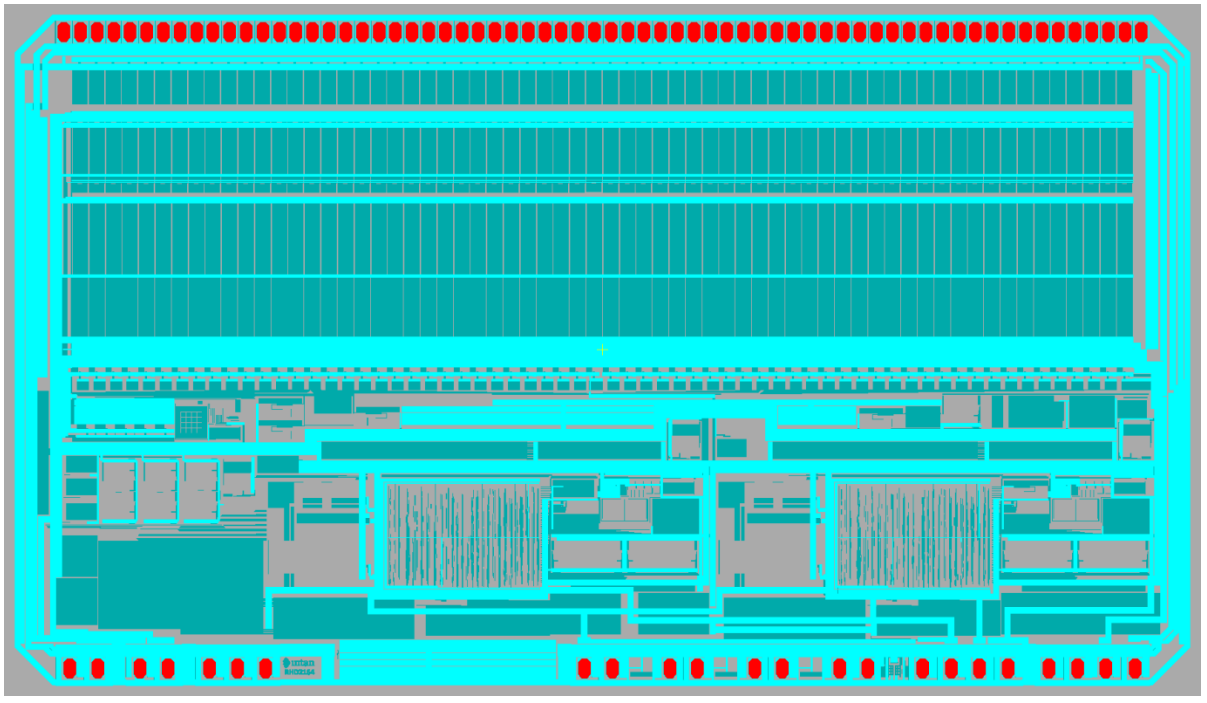
Intan Technologies RHD2164 Bare Die

Approximately 7.3 mm



Approximately 4.2 mm

Gray = approximate outline of die (may vary from die to die due to variations in sawing)

Yellow Cross = center of design (may not coincide precisely with center of die due to variations in sawing)

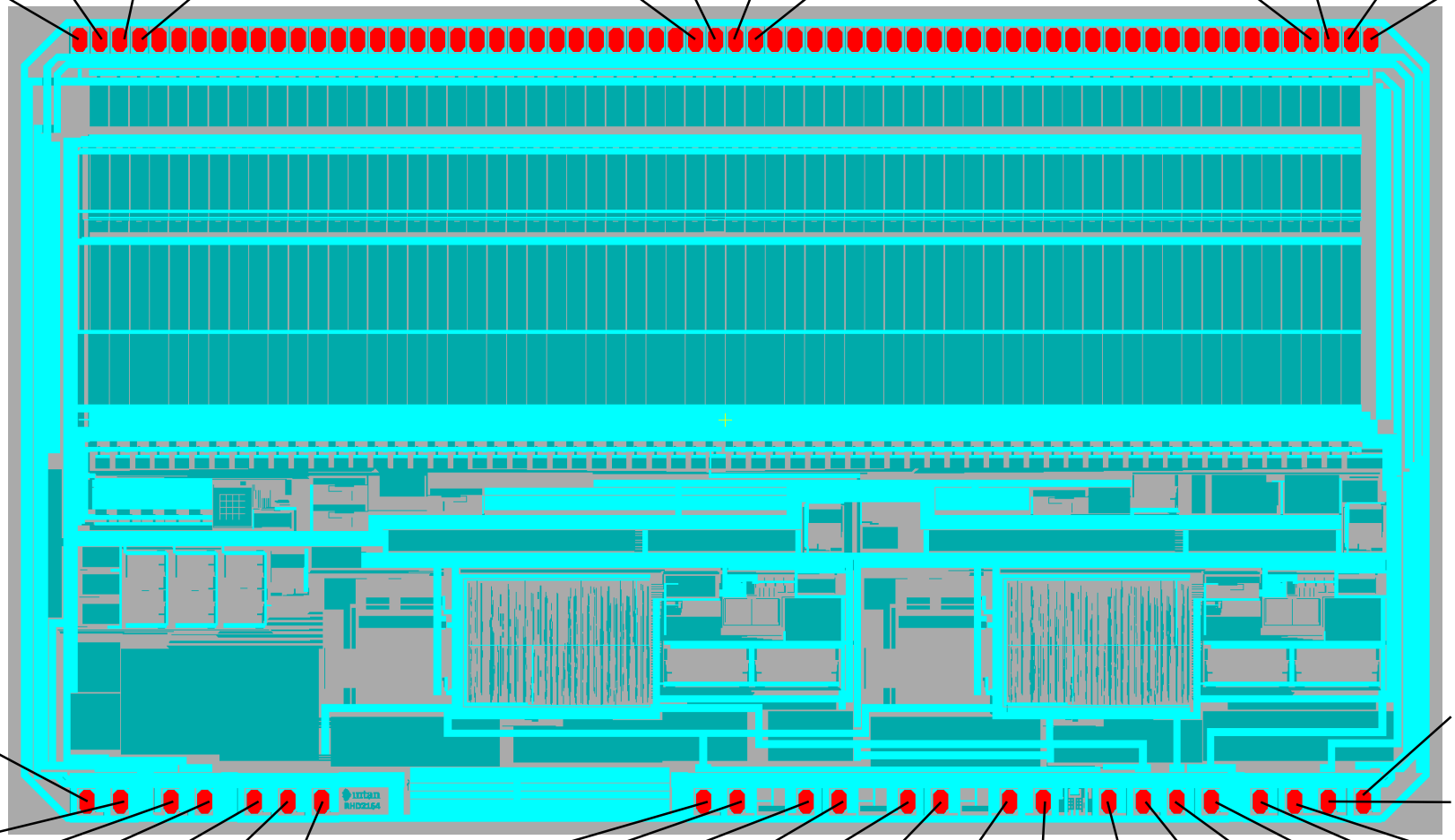
Blue, Green = top metal layers (highly visible)

Red = glass openings for bond pads

Each die is 0.20 mm (8 mils) thick

RHD2164 Coordinates of Bond Pad Centers, Relative to Center of Design

dimensions in microns



ref_elec
X = -3302.0
Y = +1945

in0
X = -3200.4
Y = +1945

in1
X = -3098.8
Y = +1945

in2
X = -2997.2
Y = +1945

amplifier pad pitch is
101.6 microns (4.000 mil)

in30
X = -152.4
Y = +1945

in31
X = -50.8
Y = +1945

in32
X = +50.8
Y = +1945

in33
X = +152.4
Y = +1945

amplifier pad pitch is
101.6 microns (4.000 mil)

in61
X = +2997.2
Y = +1945

in62
X = +3098.8
Y = +1945

in63
X = +3200.4
Y = +1945

ref_elec
X = +3302.0
Y = +1945

ref_elec
X = -3269
Y = -1945

VESD
X = -3096
Y = -1945

GND
X = -2837
Y = -1945

VDD
X = -2664
Y = -1945

auxin1
X = -2411
Y = -1945

auxin2
X = -2238
Y = -1945

auxin3
X = -2065
Y = -1945

GND
X = -112
Y = -1945

$\overline{CS}$–
X = +61
Y = -1945

$\overline{CS}$+
X = +415
Y = -1945

SCLK–
X = +580
Y = -1945

SCLK+
X = +934
Y = -1945

MOSI–
X = +1099
Y = -1945

MOSI+
X = +1453
Y = -1945

MISO–
X = +1626
Y = -1945

MISO+
X = +1964
Y = -1945

VDD
X = +2137
Y = -1945

VDD
X = +2310
Y = -1945

ADC_ref
X = +2483
Y = -1945

auxout
X = +2736
Y = -1945

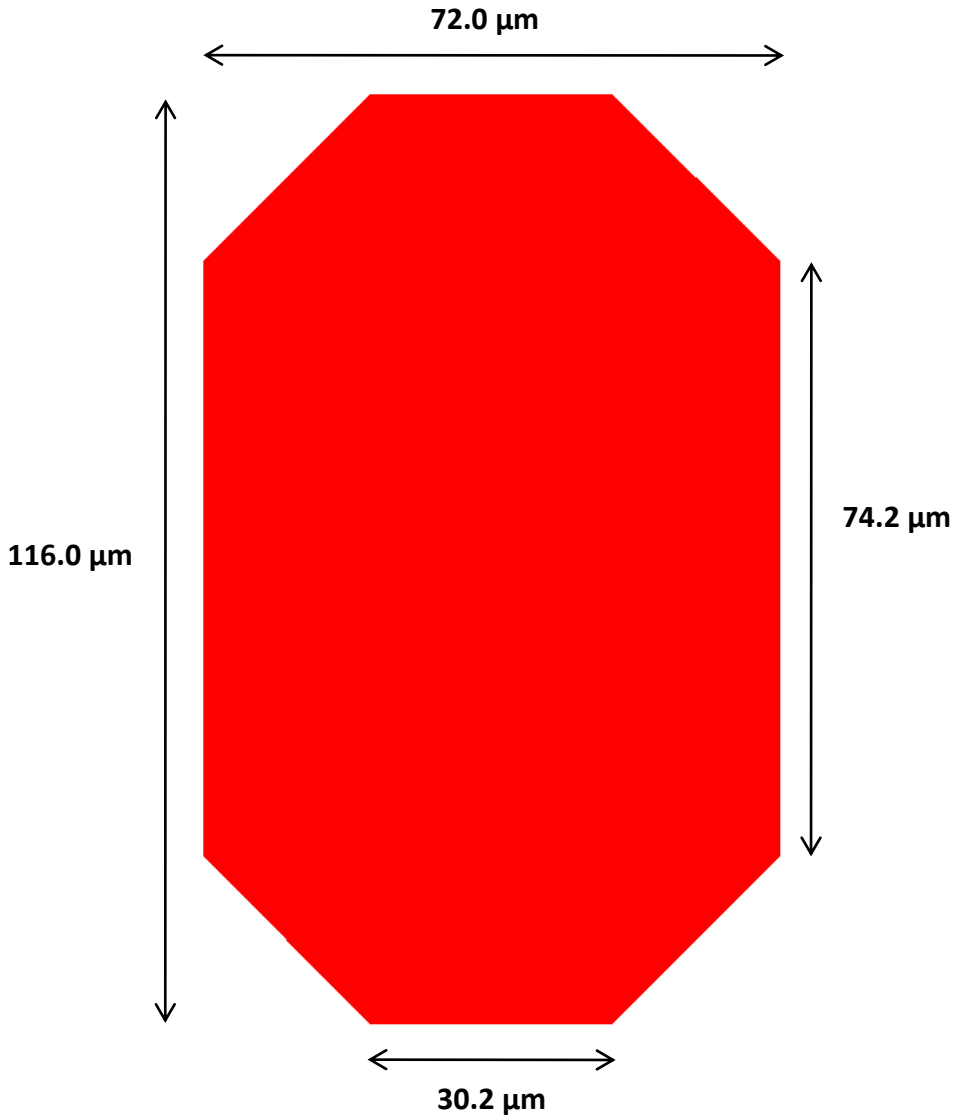
elec_test
X = +3260
Y = -1945

GND
X = +3082
Y = -1945

LVDS_en
X = +2909
Y = -1945

Bond Pad Dimensions

Bond pad metal: AlCu (99.5% aluminum, 0.5% copper)



Minimum bond pad pitch (center to center) on RHD2164: 101.6 µm (4.000 mil)

RHD2164 Notes on Optional Bond Wires

Each RHD2164 die has three bondpads for the reference electrode connection (labeled **ref_elec**). These are located in the upper left, upper right, and lower left corners of the chip. These pads are connected internally on the chip, so only **one** of these pads needs to be bonded. There is no advantage to bonding more than one of these pads. Multiple bond pads are provided only for circuit board layout convenience.

There are three ground pads and three power pads (labeled **GND** and **VDD**). **All six** of these pads **must** be bonded and connected to the appropriate supply voltages for proper operation. An off-chip 100 nF capacitor between ground and VDD should be placed less than 1 cm from the lower edge of the chip. For best operation, this capacitor should have an X5R or X7R dielectric and should be rated for at least 16V. If non-LVDS (standard CMOS) signaling is used, it is recommended that two 100 nF capacitors be used: one near the lower left corner of the chip and one near the lower right corner of the chip.

The **ADC_ref** pin must be bonded and connected to an off-chip 10 nF capacitor to ground, which should be placed within 1 cm of the lower edge the chip. This capacitor should have an X5R, X7R, C0G, or NP0 dielectric and should be rated for at least 16V. If multiple RHD2164 chips are used, each chip must have its own 10 nF capacitor. The **ADC_ref** pins of different chips should not be connected.

The **VESD** pad must be bonded and connected either to ground (recommended) or to VDD. See the "Amplifier Input Protection" section of the RHD2000 series datasheet for more information on this pin.

It is not necessary to bond the **auxin1**, **auxin2**, or **auxin3** pins if auxiliary analog signals will not be connected to the chip.

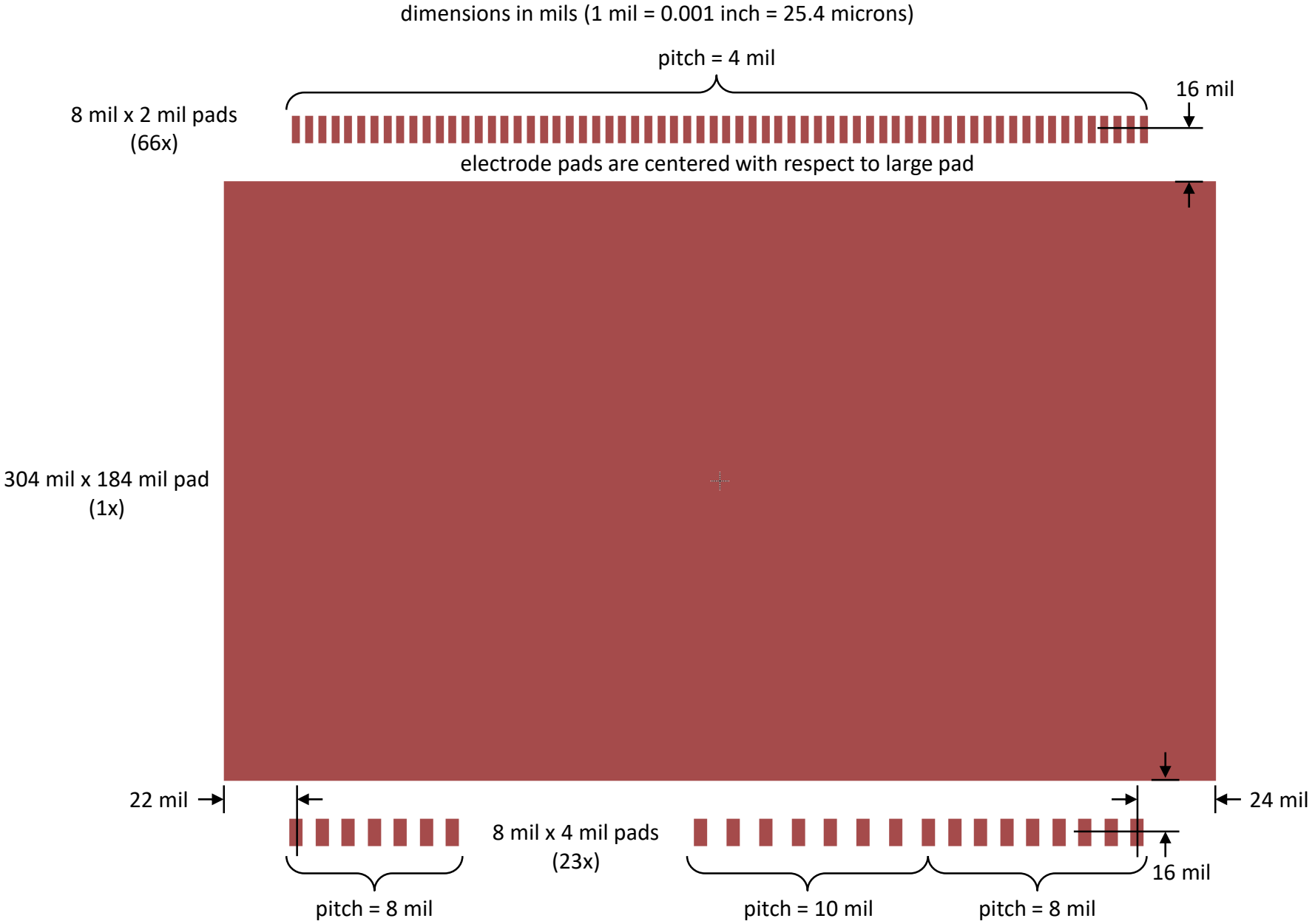
It is not necessary to bond the **auxout** pin of the auxiliary digital output will not be used.

In most applications, the **elec_test** pad should remain unbonded. This pad is typically used only to provide DC voltages for the purposes of electrode activation or electroplating. See the "Electrode Activation" section of the RHD2000 series datasheet for more details.

The **LVDS_en** pad of the RHD2164 chip has an internal pull-up resistor that enables LVDS signaling on the SPI bus if this pad is left unbonded. If non-LVDS (standard CMOS) SPI signaling is desired then this pad must be bonded and connected to ground.

If LVDS SPI signaling will be used, than all eight SPI pads (**$\overline{\text{CS}}$–**, **$\overline{\text{CS}}$+**, **SCLK–**, **SCLK+**, **MOSI–**, **MOSI+**, **MISO–**, **MISO+**) must be bonded. If non-LVDS (standard CMOS) SPI signaling will be used, the negative SPI pins (**$\overline{\text{CS}}$–**, **SCLK–**, **MOSI–**, **MISO–**) can remain unbonded.

Suggested PCB Footprint for Chip-on-Board Assembly



Immersion gold finish (ENIG) or similar planar, bondable finish should be used on PCB.